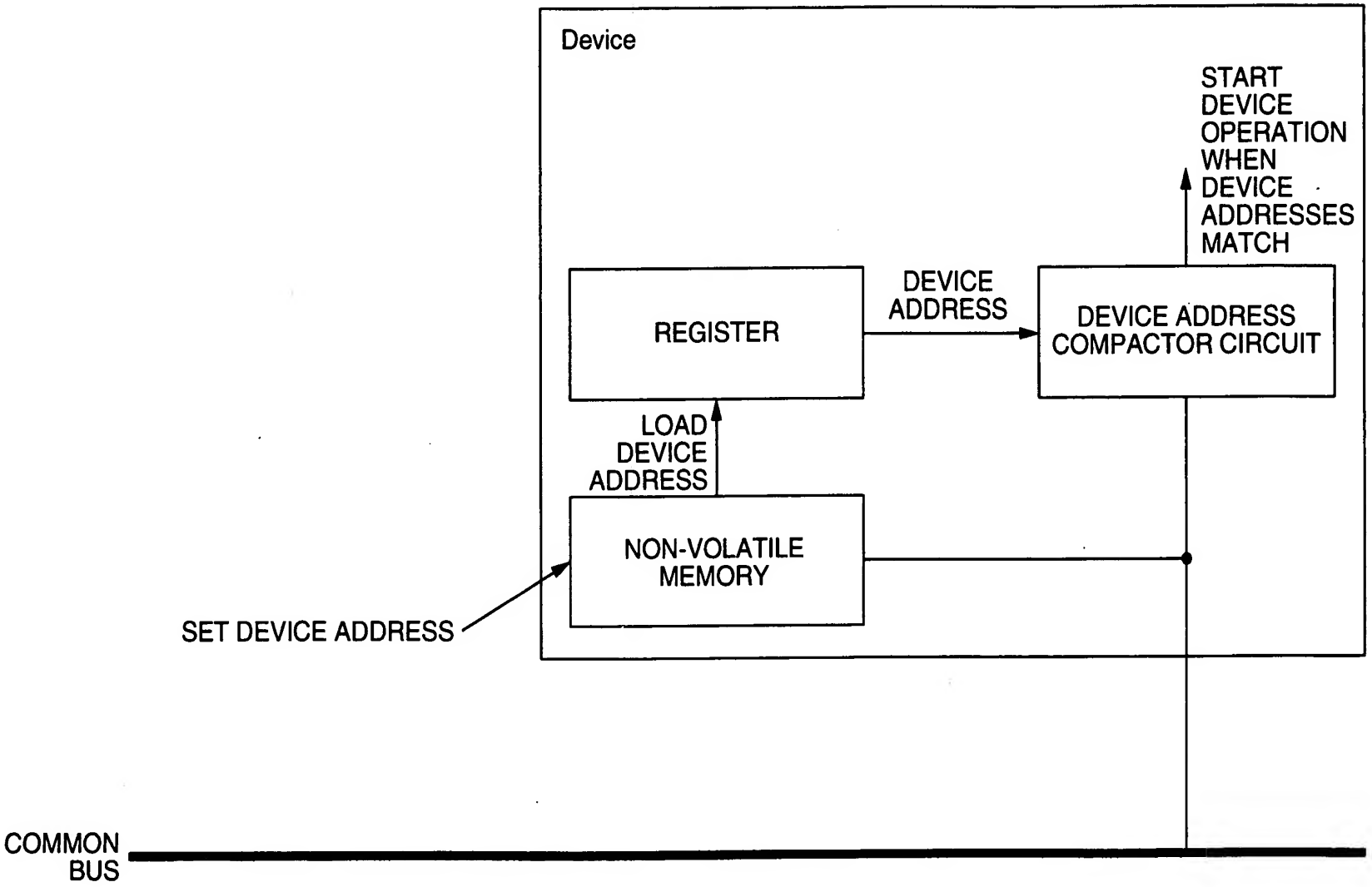
FIG. 1



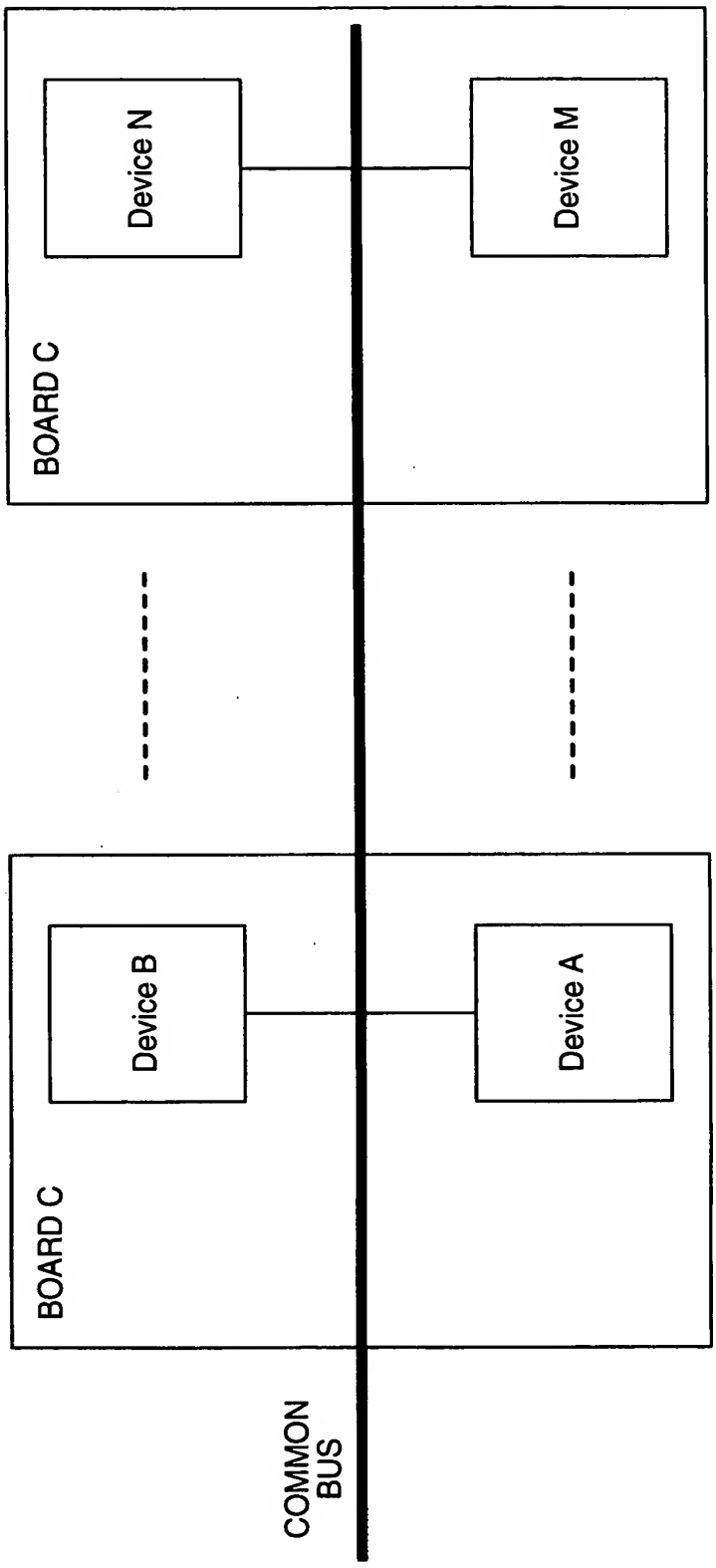


FIG. 2

FIG. 3

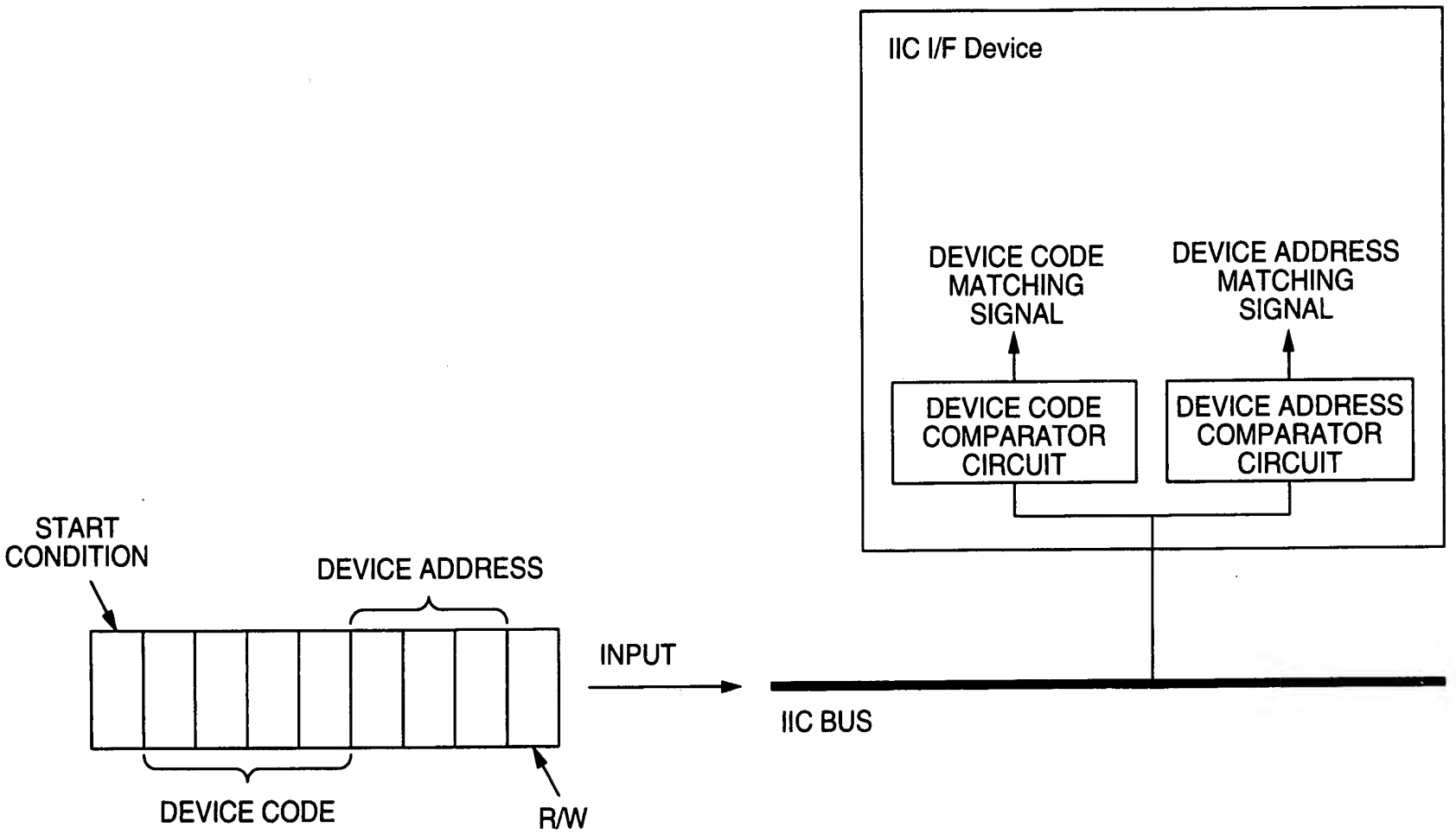

IIC I/F Device
DEVICE CODE MATCHING SIGNAL
DEVICE ADDRESS MATCHING SIGNAL
DEVICE CODE COMPARATOR CIRCUIT
DEVICE ADDRESS COMPARATOR CIRCUIT
START CONDITION
DEVICE ADDRESS
INPUT
IIC BUS
DEVICE CODE
R/W

FIG. 4

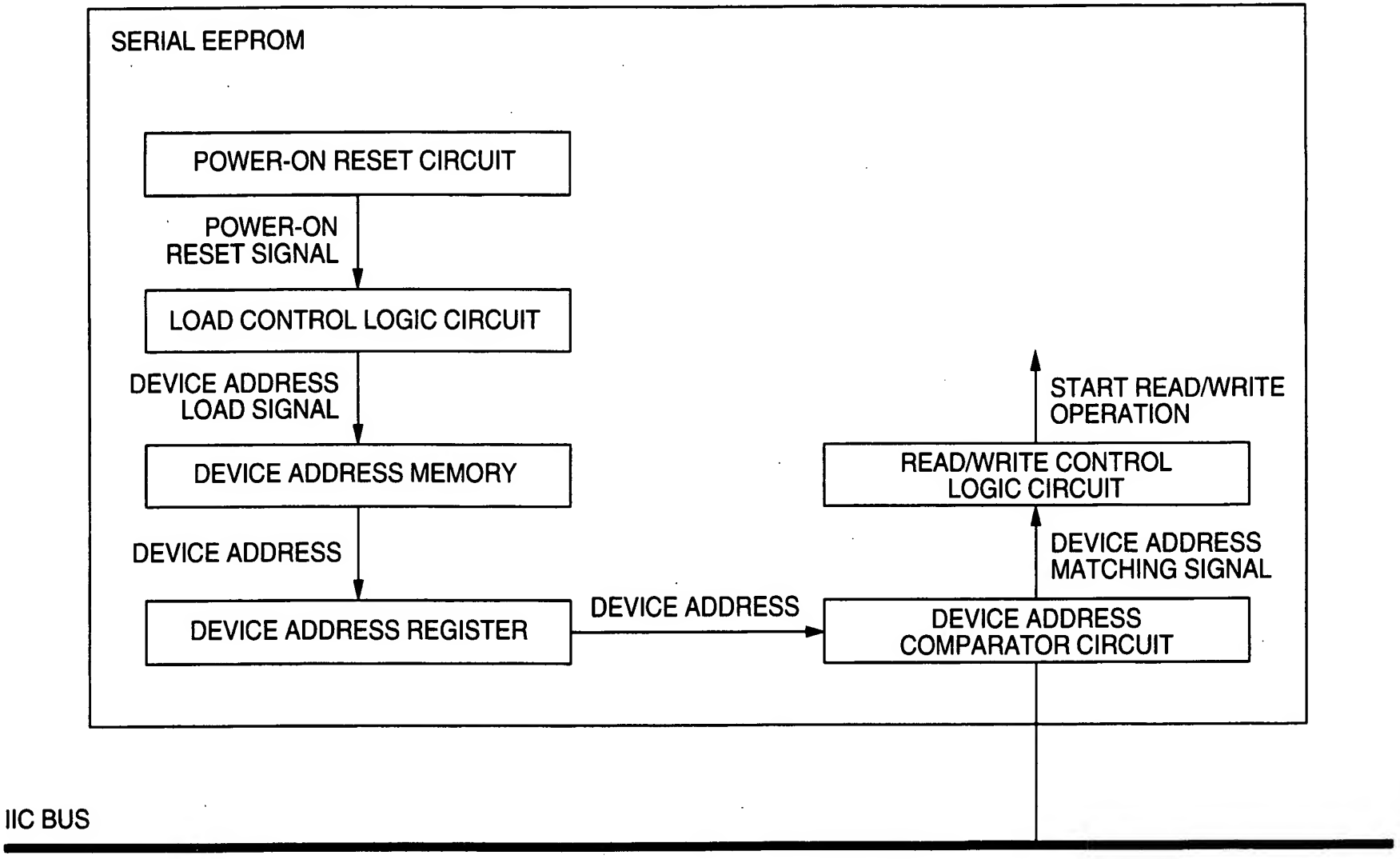


FIG. 5

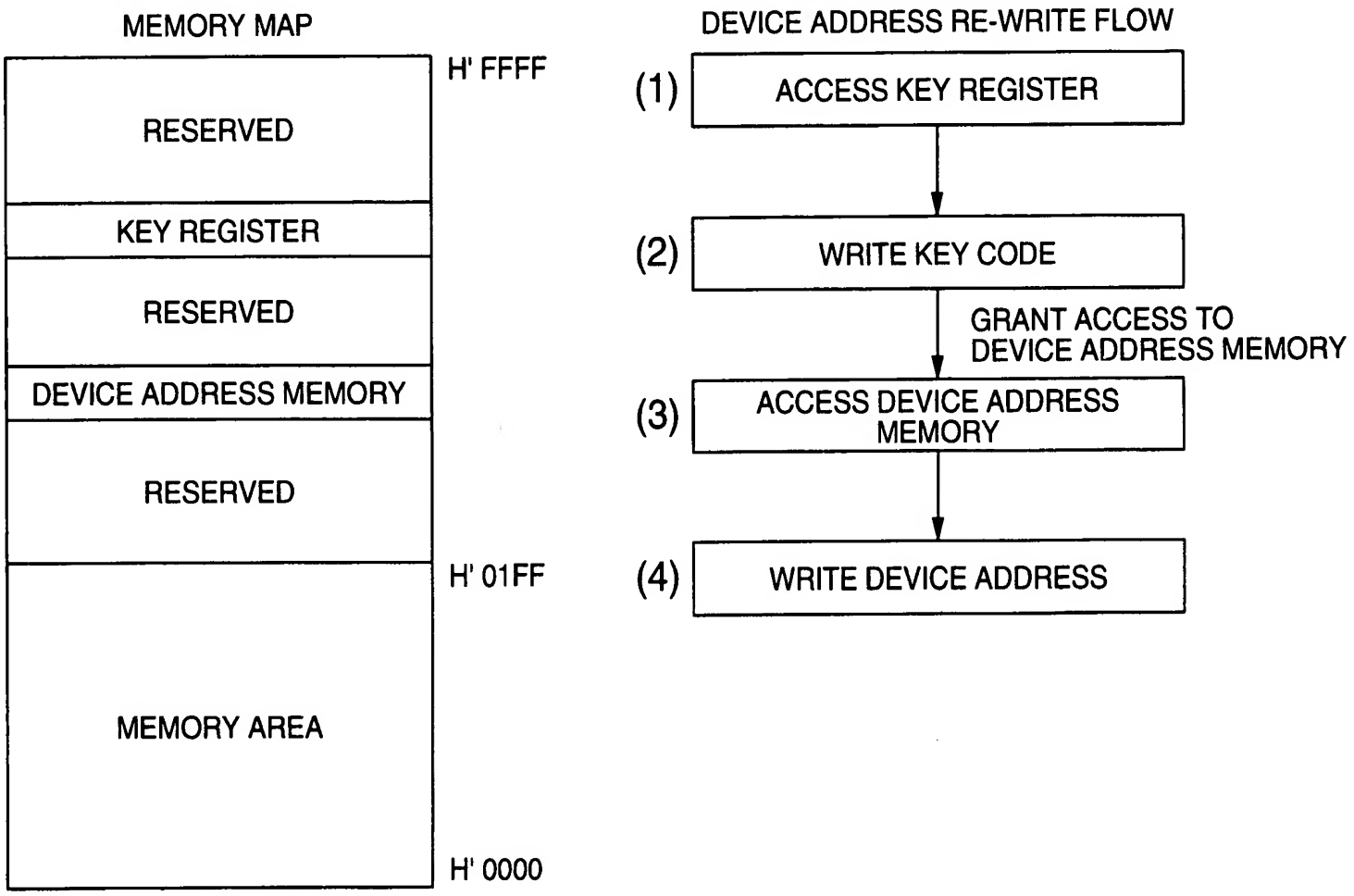


FIG. 6

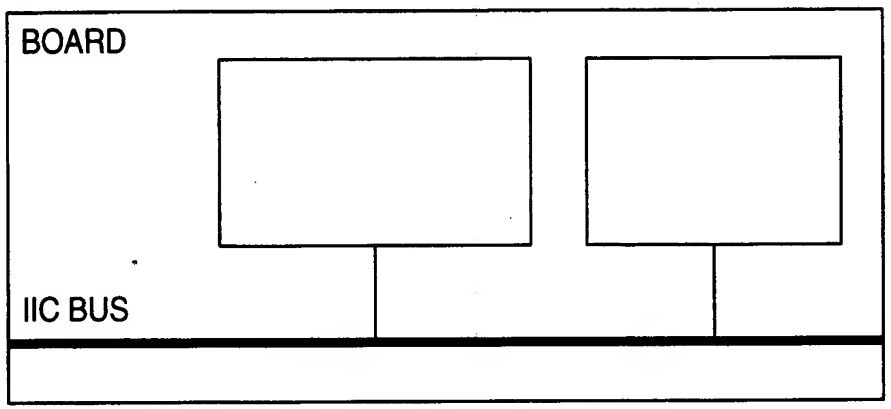


FIG. 7

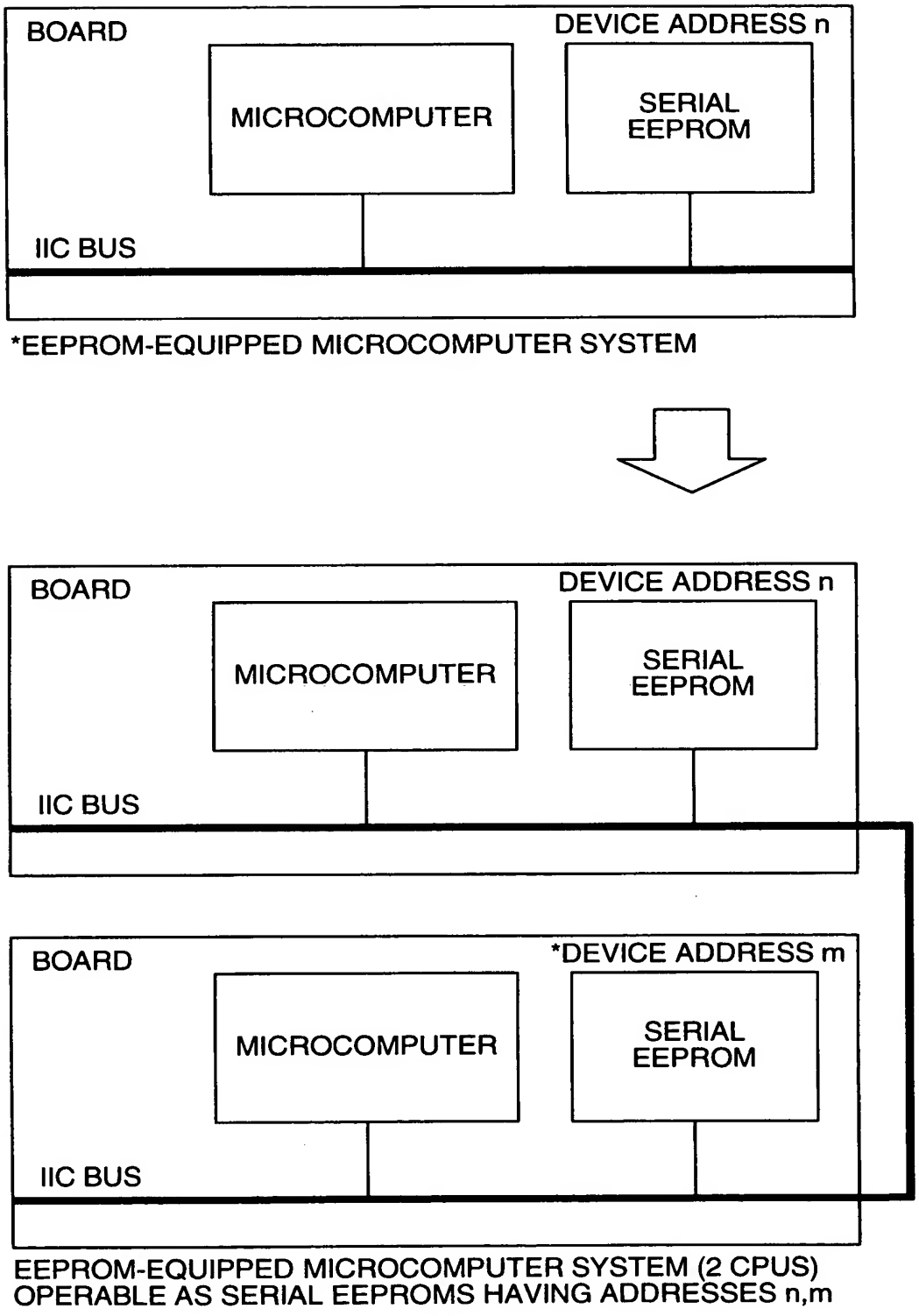
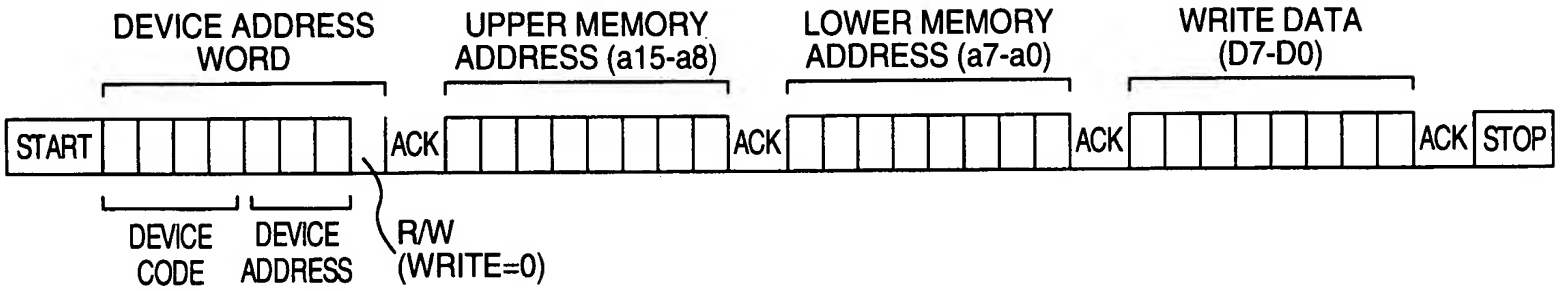

BOARD
DEVICE ADDRESS n
MICROCOMPUTER
SERIAL EEPROM
IIC BUS
*EEPROM-EQUIPPED MICROCOMPUTER SYSTEM
BOARD
DEVICE ADDRESS n
MICROCOMPUTER
SERIAL EEPROM
IIC BUS
BOARD
*DEVICE ADDRESS m
MICROCOMPUTER
SERIAL EEPROM
IIC BUS
EEPROM-EQUIPPED MICROCOMPUTER SYSTEM (2 CPUS)
OPERABLE AS SERIAL EEPROMS HAVING ADDRESSES n,m

FIG. 8

COMMUNICATION PROTOCOL (FOR WRITE OPERATION)



COMMUNICATION PROTOCOL (FOR READ OPERATION)

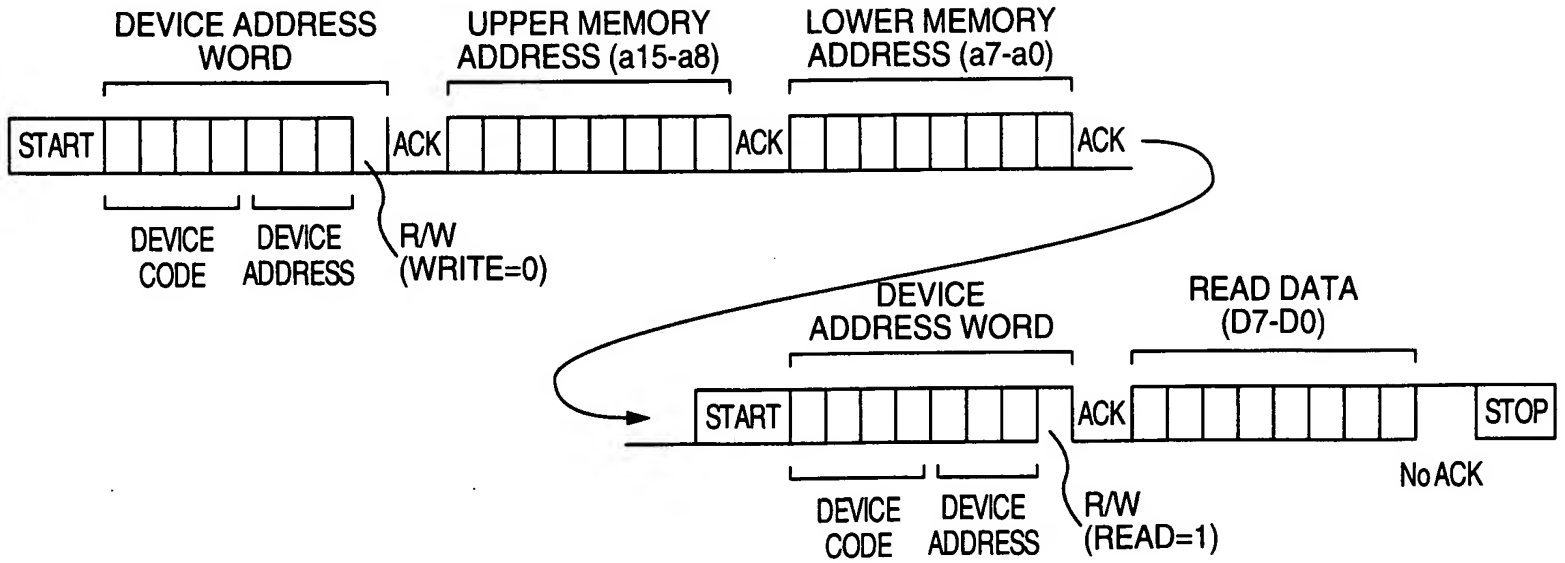
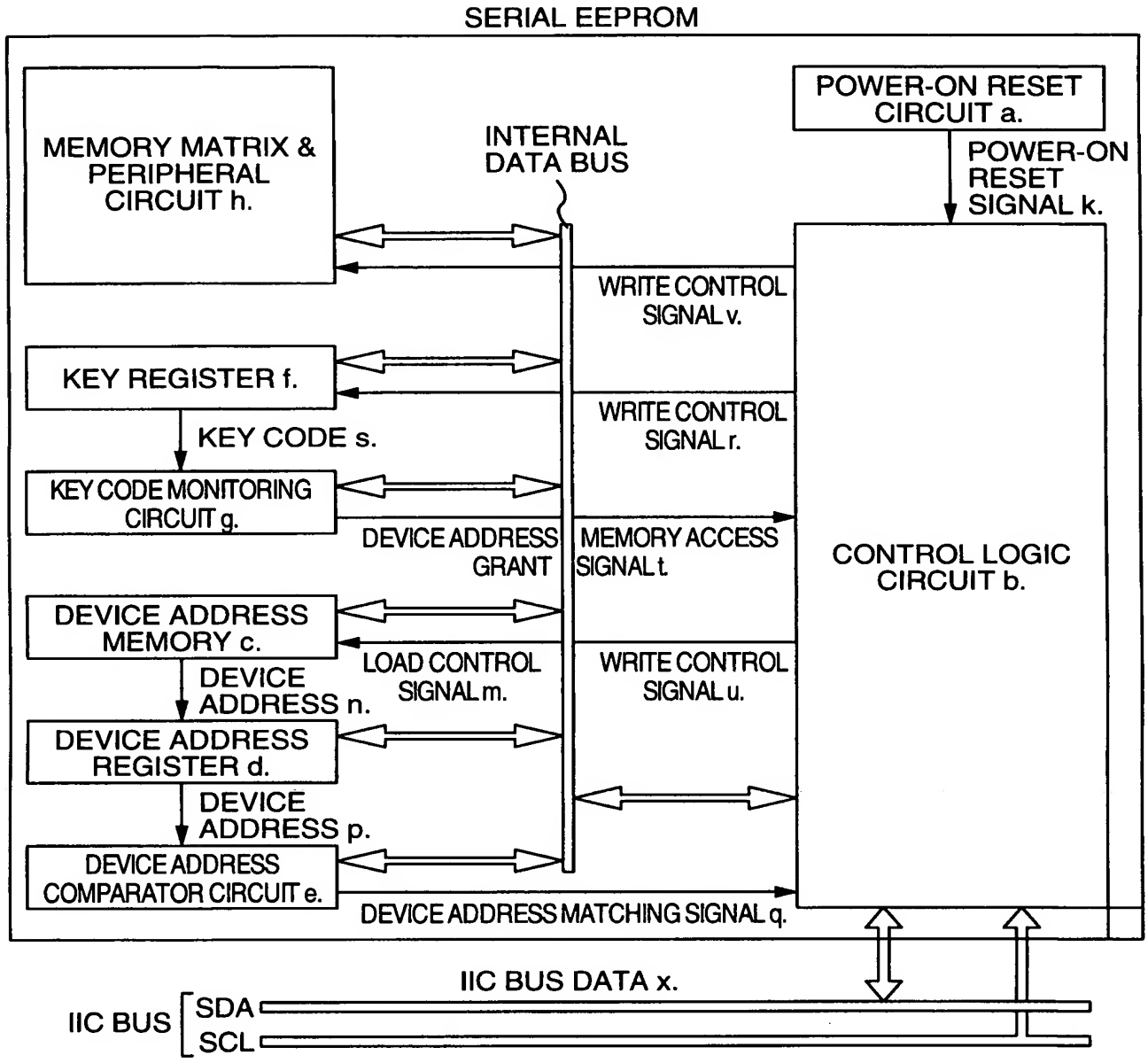


FIG. 9



IIC BUS DATA x.	DEVICE ADDRESS WORD*	UPPER MEMORY ADDRESS	LOWER MEMORY ADDRESS	WRITE DATA
1	10100000	H' FF	H' 10	KEY CODE
2	10100000	H' FF	H' 09	xxxxx101
3	10101010	H' 00	H' 00	WRITE DATA

FIG.10

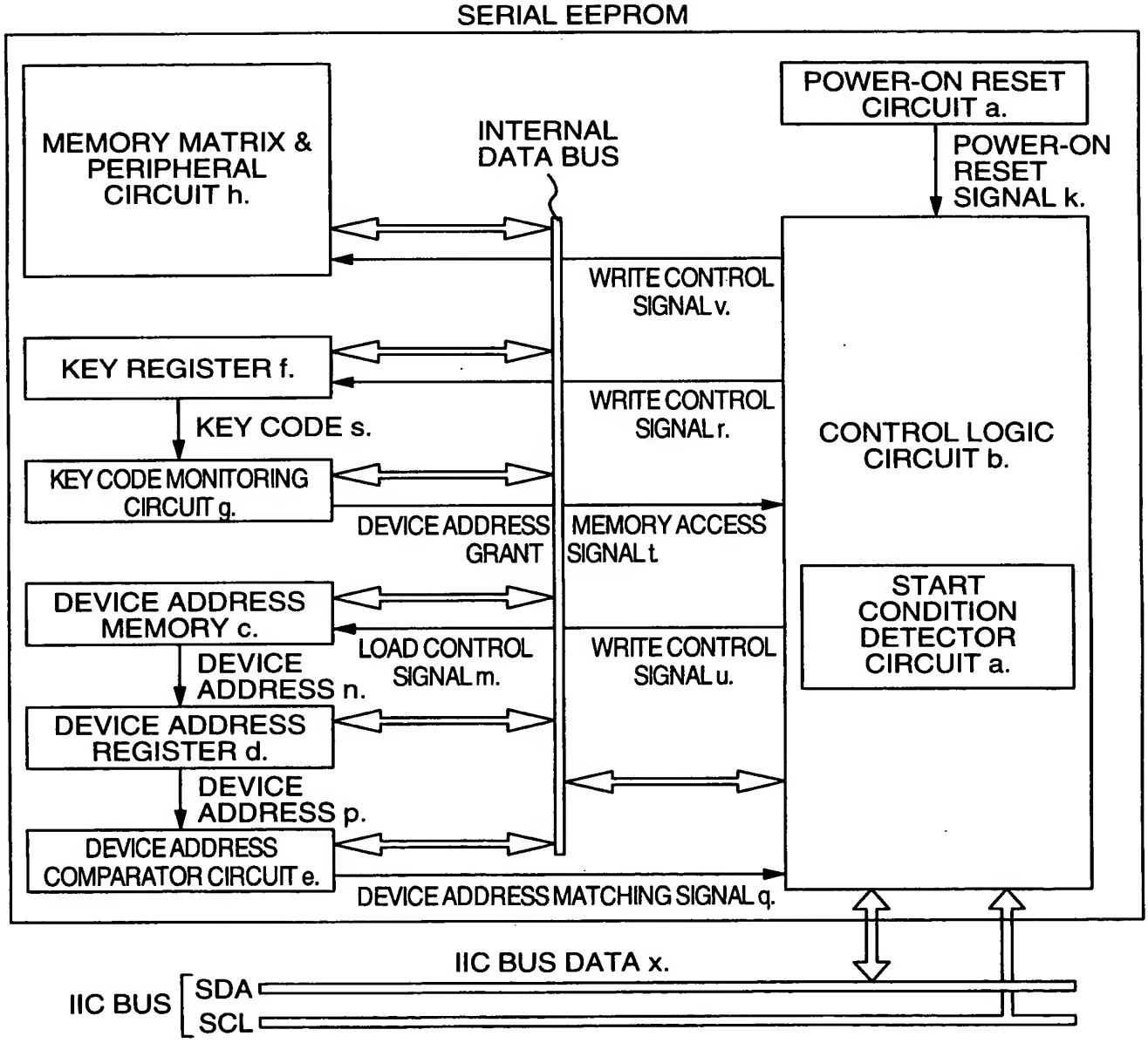

SERIAL EEPROM
MEMORY MATRIX & PERIPHERAL CIRCUIT h.
INTERNAL DATA BUS
POWER-ON RESET CIRCUIT a.
POWER-ON RESET SIGNAL k.
WRITE CONTROL SIGNAL v.
KEY REGISTER f.
WRITE CONTROL SIGNAL r.
KEY CODE s.
CONTROL LOGIC CIRCUIT b.
KEY CODE MONITORING CIRCUIT g.
DEVICE ADDRESS GRANT
MEMORY ACCESS SIGNAL t.
START CONDITION DETECTOR CIRCUIT a.
DEVICE ADDRESS MEMORY c.
LOAD CONTROL SIGNAL m.
WRITE CONTROL SIGNAL u.
DEVICE ADDRESS n.
DEVICE ADDRESS REGISTER d.
DEVICE ADDRESS p.
DEVICE ADDRESS COMPARATOR CIRCUIT e.
DEVICE ADDRESS MATCHING SIGNAL q.
IIC BUS DATA x.
IIC BUS
SDA
SCL

FIG. 11

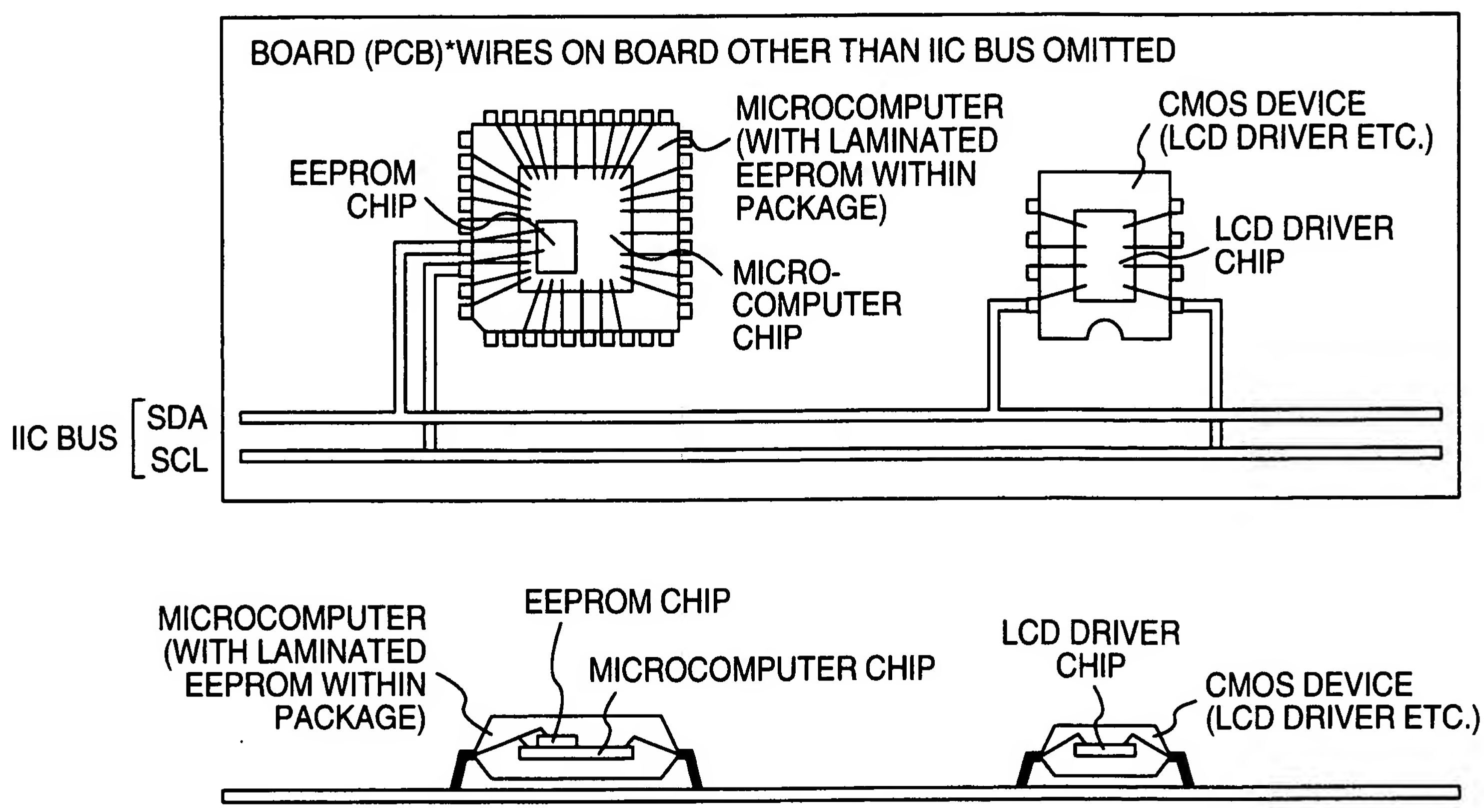
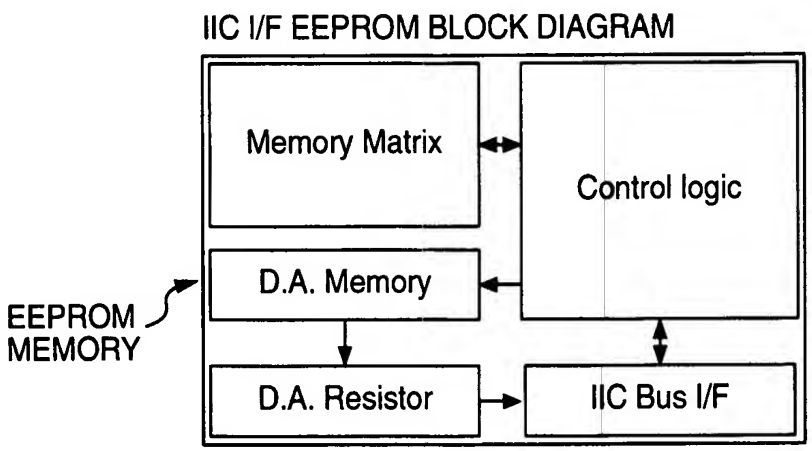

BOARD (PCB)*WIRES ON BOARD OTHER THAN IIC BUS OMITTED
EEPROM CHIP
MICROCOMPUTER (WITH LAMINATED EEPROM WITHIN PACKAGE)
MICRO-COMPUTER CHIP
CMOS DEVICE (LCD DRIVER ETC.)
LCD DRIVER CHIP
IIC BUS
SDA
SCL
MICROCOMPUTER (WITH LAMINATED EEPROM WITHIN PACKAGE)
EEPROM CHIP
MICROCOMPUTER CHIP
LCD DRIVER CHIP
CMOS DEVICE (LCD DRIVER ETC.)

FIG. 12



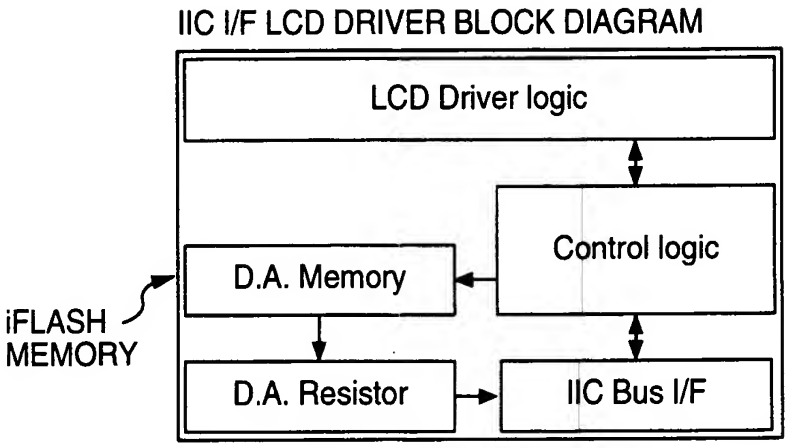
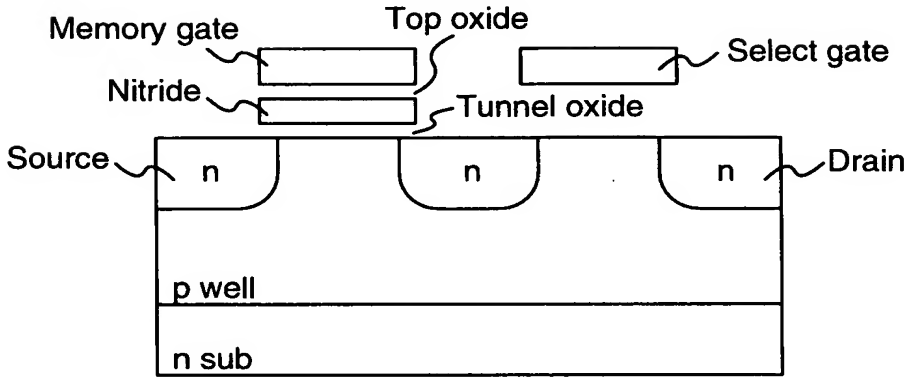
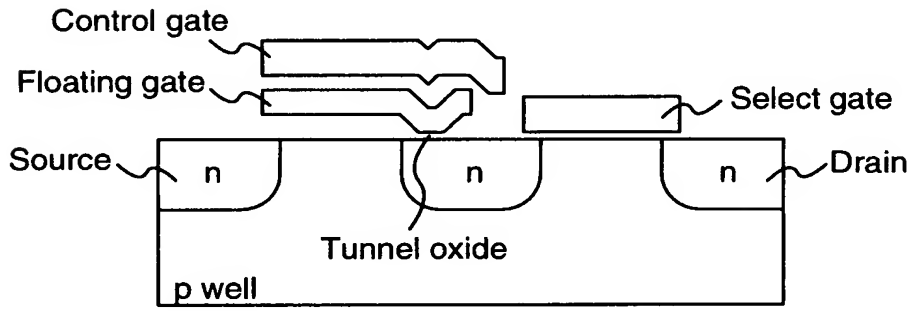


FIG. 13

MONOS MEMORY CELL



FLOTOX MEMORY CELL



iFLASH MEMORY CELL

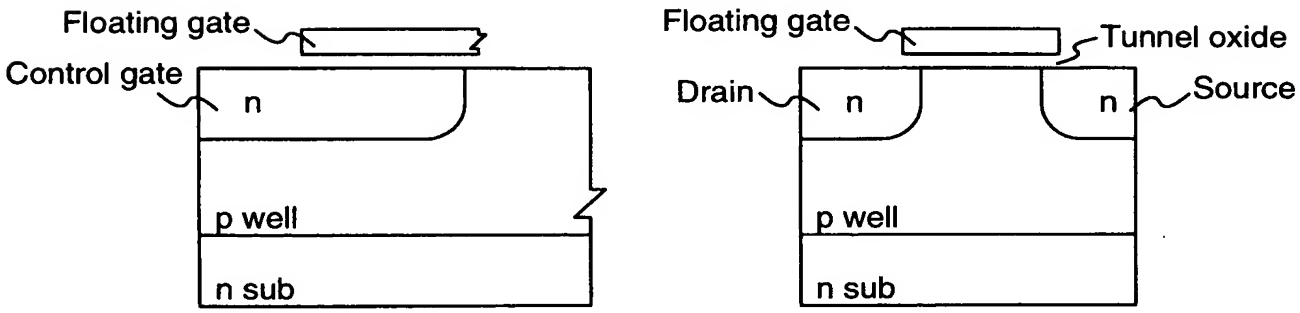


FIG. 14

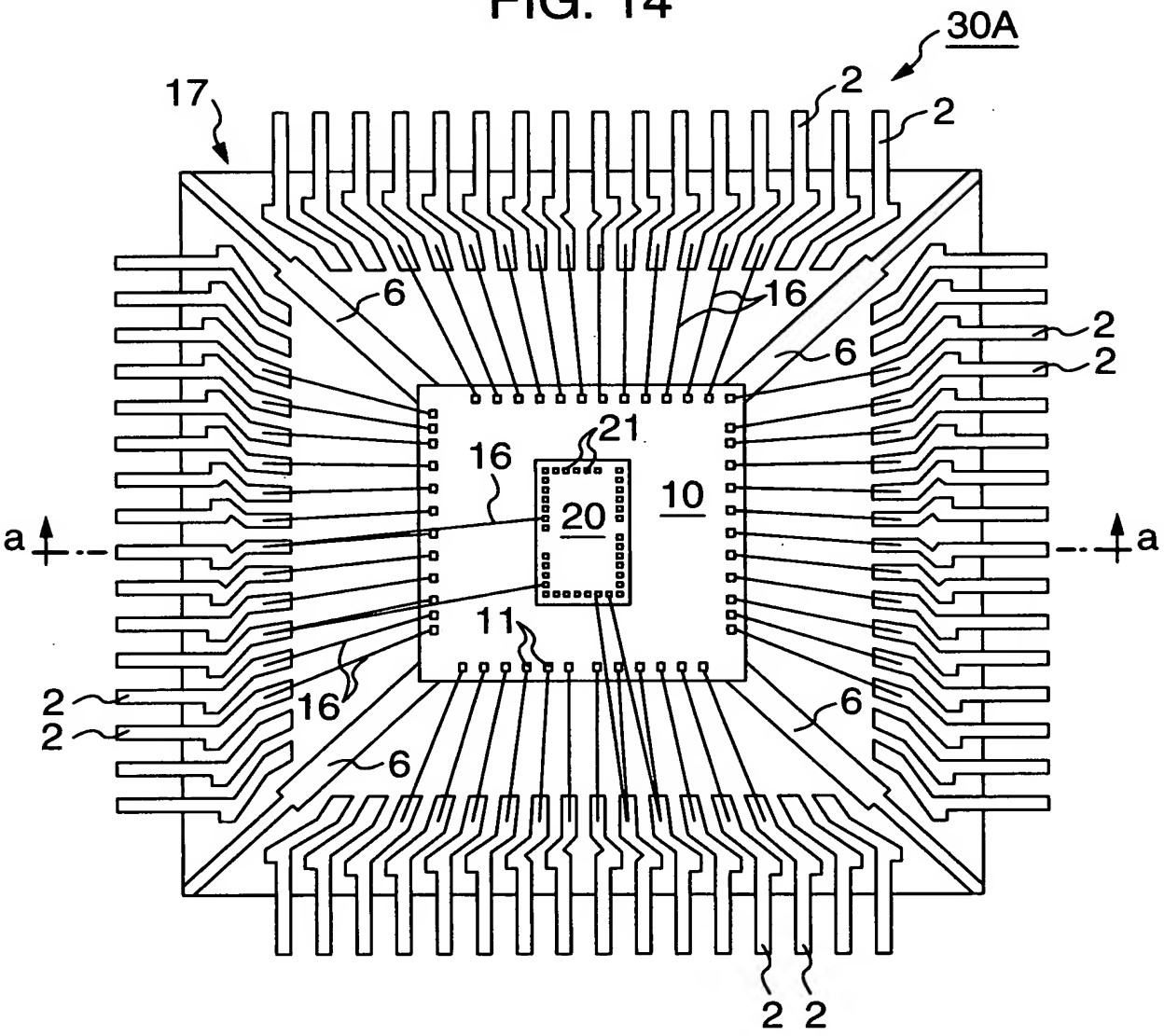


FIG. 15

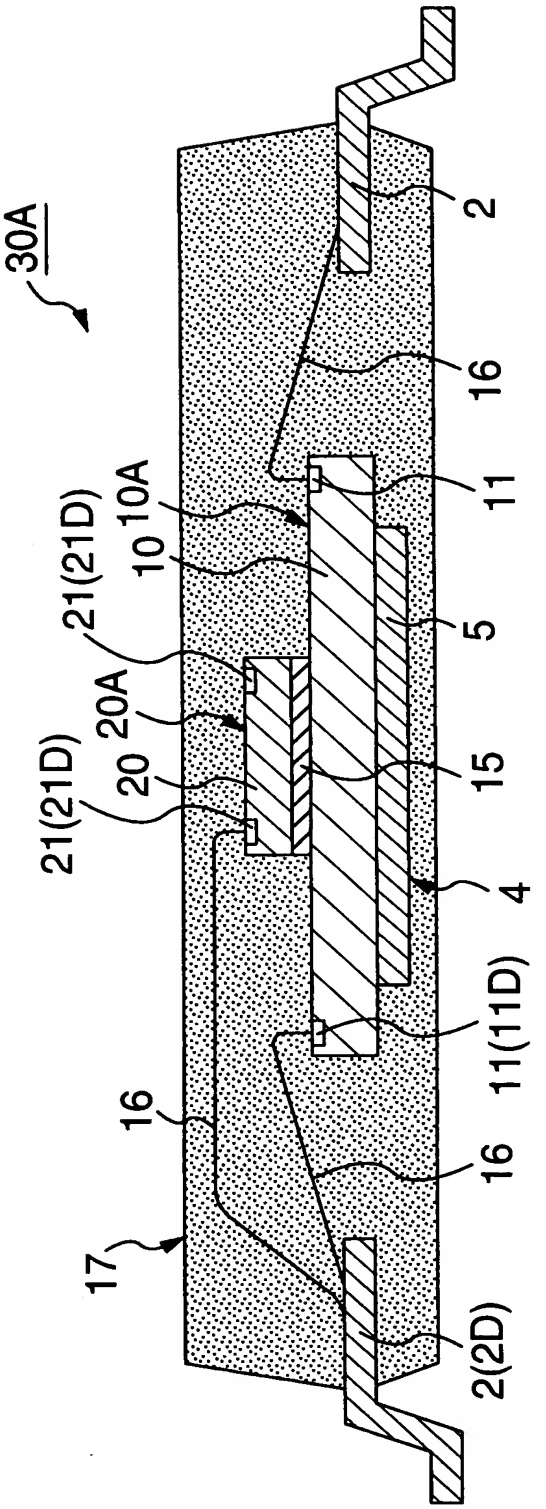


FIG. 16

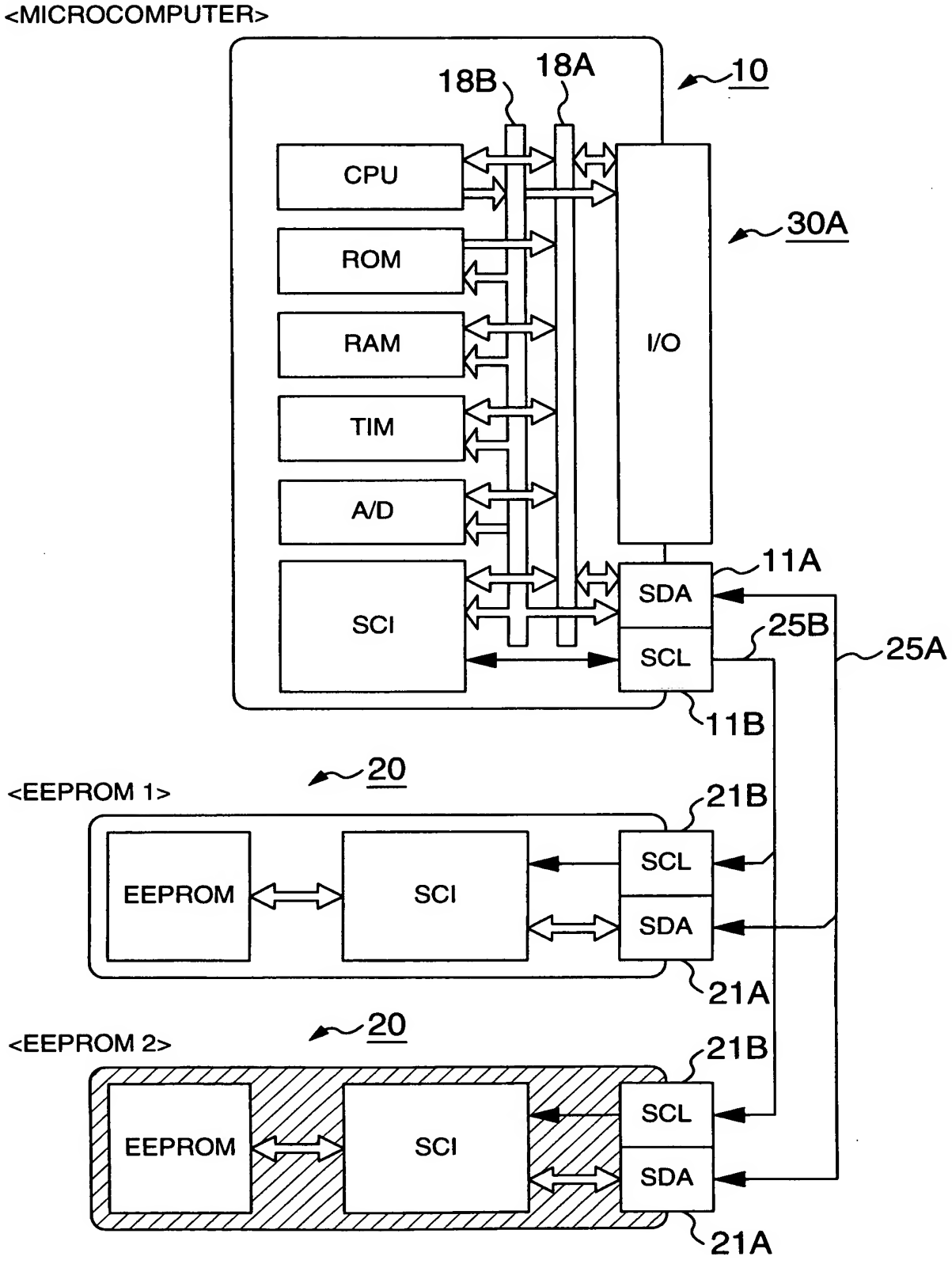

<MICROCOMPUTER>
18B
18A
10
CPU
ROM
RAM
TIM
A/D
SCI
I/O
30A
11A
SDA
SCL
25B
25A
11B
20
<EEPROM 1>
21B
EEPROM
SCI
SCL
SDA
21A
20
<EEPROM 2>
21B
EEPROM
SCI
SCL
SDA
21A

FIG. 17

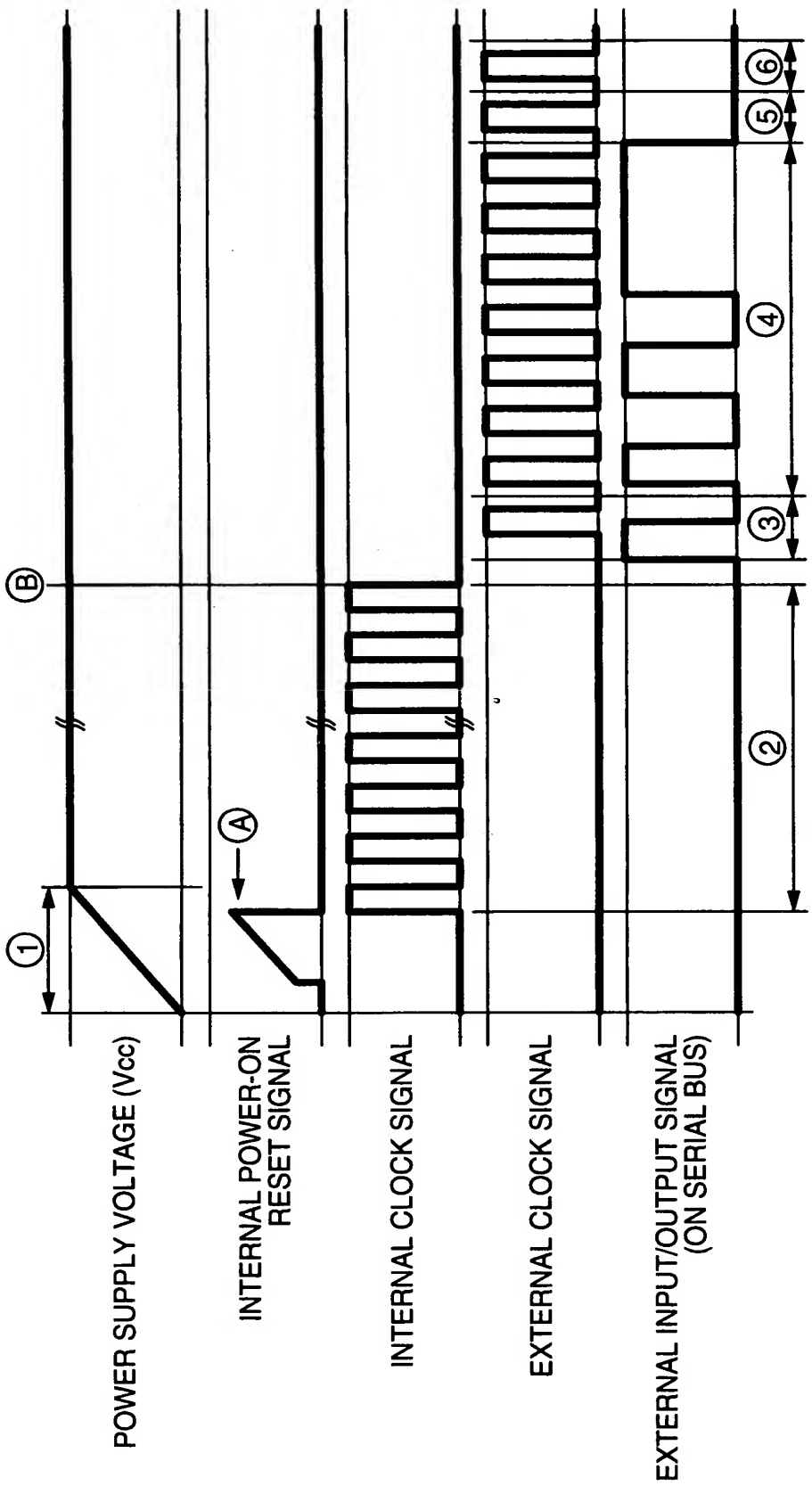

POWER SUPPLY VOLTAGE (Vcc)
INTERNAL POWER-ON RESET SIGNAL
INTERNAL CLOCK SIGNAL
EXTERNAL CLOCK SIGNAL
EXTERNAL INPUT/OUTPUT SIGNAL (ON SERIAL BUS)
①
②
③
④
⑤
⑥
Ⓐ
Ⓑ

FIG. 18

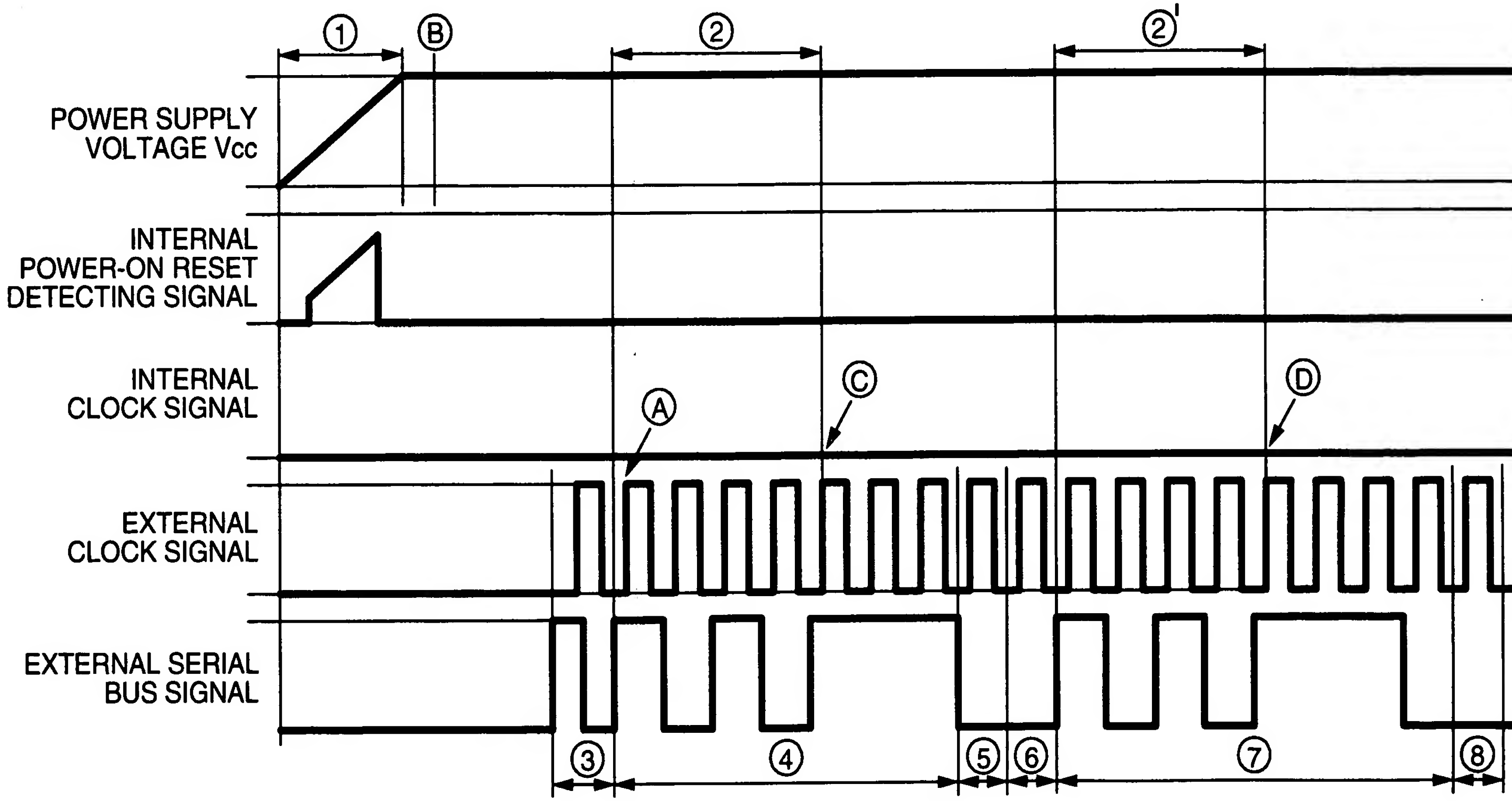
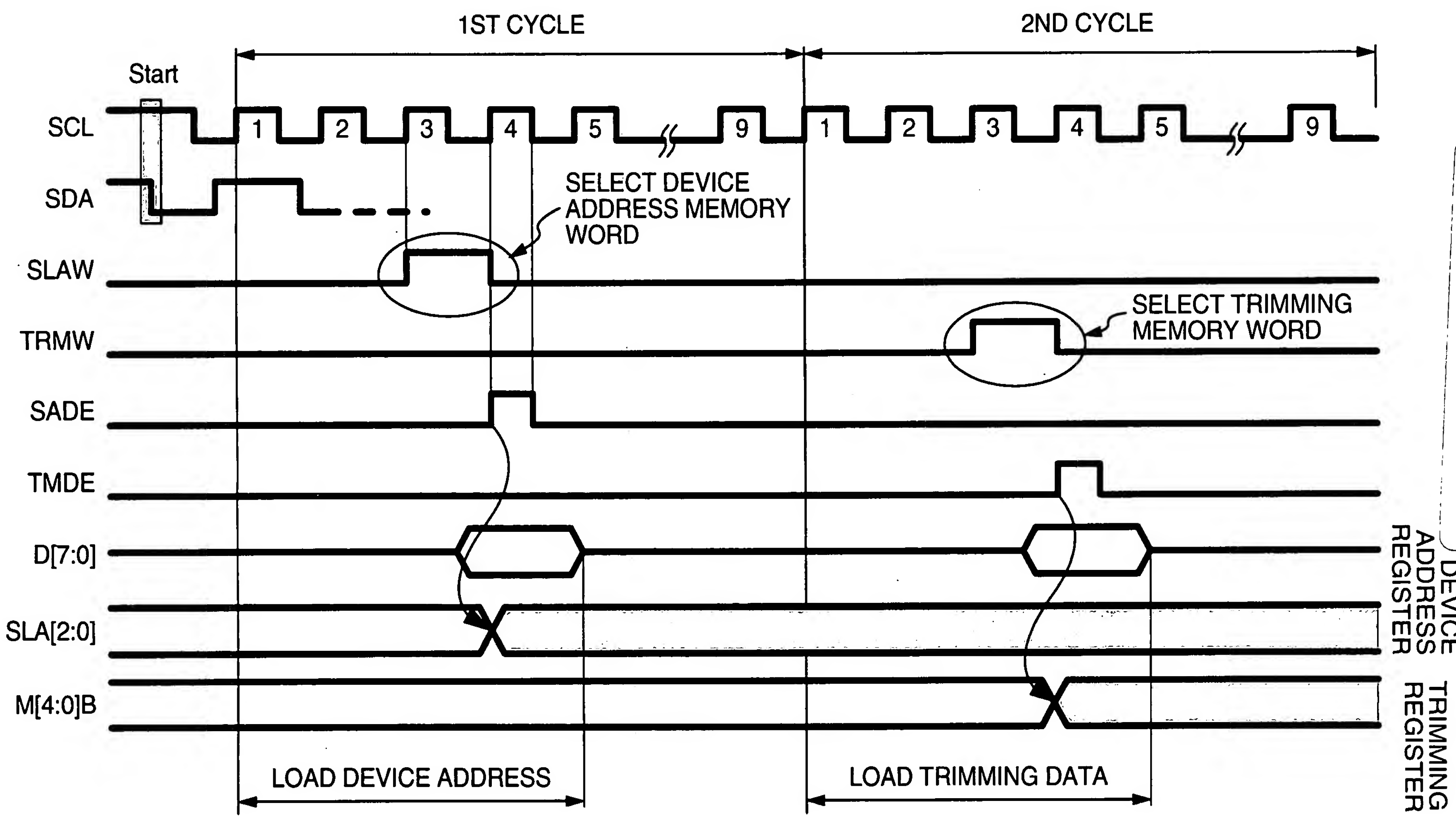

POWER SUPPLY VOLTAGE Vcc
INTERNAL POWER-ON RESET DETECTING SIGNAL
INTERNAL CLOCK SIGNAL
EXTERNAL CLOCK SIGNAL
EXTERNAL SERIAL BUS SIGNAL
①
Ⓑ
②
②'
Ⓐ
Ⓒ
Ⓓ
③
④
⑤
⑥
⑦
⑧

FIG. 19


1ST CYCLE
2ND CYCLE
Start
SCL
SDA
SLAW
TRMW
SADE
TMDE
D[7:0]
SLA[2:0]
M[4:0]B
1
2
3
4
5
9
SELECT DEVICE ADDRESS MEMORY WORD
SELECT TRIMMING MEMORY WORD
DEVICE ADDRESS REGISTER
TRIMMING REGISTER
LOAD DEVICE ADDRESS
LOAD TRIMMING DATA